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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,965	07/18/2003	Ming-Cheng Chang	10112501	4018

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EXAMINER	
GOUDREAU, GEORGE A	

ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,965	CHANG ET AL.	
	Examiner	Art Unit	
	George A. Goudreau	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

George A Goudreau

GEORGE GOUDREAU
PRIMARY EXAMINER
6-05

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 9-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

-In the claims, the usage of the term "predetermined" is vague, and indefinite.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5, 9-10, 12-13, 15-16, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et. al. (6,909,136).

Chen et. al. disclose a deep trench self-alignment process for an active area of a partial vertical cell which is comprised of the following steps:

-Deep trenches (111) are rie etched into a semiconductor substrate using a pad Si3N4 layer, pad SiO2 layer, or pad SiO2/Si3N4 layer as an etch mask.;

-A storage node (14) of a deep trench capacitor is formed using a first conductive layer.;

-A second conductive layer (18) which is encased in a collar oxide layer (16) is formed in the deep trench.;

-A third conductive layer (19) is formed in the deep trench.;

-A TTO layer (21), which is comprised of trench top oxide layer, is formed in the deep trench on top of the deep trench capacitor.;

-A sacrificial antireflective layer (22) which constitutes a type of etch mask is formed in the deep trench.;

-A photo resist etch mask (30) is formed onto the surface of the wafer.; and

-The semiconductor substrate is etched to below the level of the TTO layer (21) to leave behind a silicon pillar (412) structure. The photo resist etch mask, and sacrificial layer act as an etch mask during this step.

This is discusses specifically in columns 3-5; and discussed in general in columns 1-8. This is shown in figures 1-18.

4. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

5. Claims 1-3, 5, and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Gruening et. al. (6,204,140).

Gruening et. al. disclose a deep trench self-alignment process for an active area of a partial vertical cell which is comprised of the following steps:

-A deep trench is etched into a cz-Si wafer (16) using a patterned pad Si3N4 layer (32) as an etch mask.;

-A polysi capacitor (24) is formed inside a deep trench which is lined with a collar SiO2 layer (18).;

-A SiON antireflective layer (44) is used to planarize the surface of the wafer.

The SiON layer functions as a type of etch mask.;

-A photo resist etch mask (48) is formed onto the surface of the SiON layer (44).;

-The SiON layer is anisotropically rie etched using the patterned photo resist etch mask.;

-The polysi layer (42), and the cz-Si wafer (16) is anisotropically rie etched using the SiON AR film (44), and the photo resist film (48) as an etching mask.

This is discussed specifically in columns 3-6; and discussed in general in columns 1-10. This is shown in figures 1-10.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 7-8, 10-11, 14, and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et. al. as applied in paragraph 3 above.

Chen et. al. as taught in paragraph 3 above fail to disclose the following aspects of applicant' s claimed invention:

-the specific anisotropic rie etching of the silicon material to leave behind a pillar structure in the process taught above; and

-the specific spacing between the deep trench capacitors which is claimed by the applicant

It would have been obvious to one skilled in the art to anisotropically rie etch the silicon material in the process taught above to leave behind a pillar structure based upon the following. The usage of a rie etching process to anisotropically etch a Si material is conventional or at least well known in the etching arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for patterning the pillar structure in the process taught above to the means which are specifically taught above.

It would have been obvious to one skilled in the art to space the deep trench capacitors in the semiconductor wafer with the specific spacing, which are claimed by the applicant based upon the following. It would have been desirable to space the deep trench capacitors as closely as possible to maximize the usage of expensive real estate on the chip without spacing the deep trench capacitors to closely to each other such that they electrically interfere with the operation of one another.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gruening et. al. as applied in paragraph 5 above.

Gruening et. al. as applied in paragraph 5 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of a plasma comprised of (HBr-O2) to anisotropically rie etch the polysi, and cz-Si layer selectively to SiON in the etching process taught above

It would have been obvious to one skilled in the art to employ a plasma comprised of (HBr-O2) to anisotropically rie etching the silicon layers selectively to the SiON etch mask in the process taught above based upon the following. It is conventional or at least well known in the semiconductor processing arts to use a plasma comprised of (HBr-O2) to anisotropically rie etch silicon layers selectively to a SiON etch mask. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for conducting the etching process taught above to the specific means, which are taught above.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication should be directed to examiner George A. Goudreau at telephone number (571)-272-1434.

George A. Goudreau
Primary Examiner
Art Unit 1763